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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,285	MUNGUIA ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-32,35-42 and 45-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-32, 35-42, 45-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413), Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6 August 2007 has been entered.

Status of Claims

2. Claims 24-32, 35-42 and 45-47 are pending in the Application.

Claims 1-23, 33, 34, 43, 44, 48 and 49 are cancelled.

Claims 24, 30, 32, 37, 38, 41 and 47 are amended.

Claims 24-32, 35-42 and 45-47 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 6 August 2007 in response to the office action mailed on 4 April 2007 have been fully considered, but they are moot in view of the new grounds of rejection discussed *infra*.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 24-32, 35-42 and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al. (US Patent 6,199,151 B1), hereinafter Williams, and in further view of Fallon et al. (US Patent 7,181,606 B2), hereinafter Fallon.

As for claim 24, Williams teaches an apparatus (Fig. 1, element 10) comprising:

a controller (Fig. 1, element 4, TLB table, address decode logic, chip select logic), before controller initialization in response to a power-up or a soft reset of the apparatus (col. 5, lines 36-58 – memory addressing and mapping is determined at power-up), configured to generate

an unencoded chip select word (chip select - Fig. 3, CS: bits 8-1) in response to an address for a memory device, wherein the unencoded chip select word comprises the lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the memory device (the device row is selected by asserting one of the eight chip select bits, and de-asserting the remaining seven. When relying on the unencoded chip select word, all eight bits (including the lowest order)

are required to appropriately select the row) – col. 5, line 59 through col. 6, line 6;

an encoded chip select word (chip select - Fig. 3, CS: bits 2-0) in response to an address for a memory device, wherein the encoded chip select word comprises the lowest order active chip select bit that corresponds to a predetermined chip-select line used to select the memory device (the row value is selected by asserting one or more of the three encoded select bits. When relying on the encoded chip select word, all thee bits (including the lowest order) are required to appropriately select the row) – col. 6, lines 7-26; and

wherein the encoded chip select word and the unencoded chip select word select a same memory device (both the encoded and unencoded chip selects are relied upon to select rows within the same device – col. 6, lines 33-50).

Despite these teachings, Williams fails to teach his memory device as a boot device as recited by Applicant in this claim.

Fallon however teaches a system and method for accelerated loading of operating systems and application programs, which stores boot information in memory devices. The information is loaded and subsequently used to boot the system and load application programs – col. 3, lines 34-52.

As for claim 32, though William's teaches his memory devices and storing data, he fails to specifically teach the devices as storing a boot code nub.

Fallon however teaches a system and method for accelerated loading of operating systems and application programs, which stores boot information (boot code nub) in memory devices. The information is loaded and subsequently used to boot the system and load application programs – col. 3, lines 34-52.

Claims 38, 41 and 47 are directed to a system, method and medium respective, and are similar in scope to claim 32; therefore these claims are rejected based on the same rationale as claims 24 and 32, *supra*.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Williams to further include Fallon's system and method for accelerated loading of operating systems and application programs into his own system and method for storing a device row indicator for use in a subsequent page-miss memory cycle. By doing so, Williams could exploit the benefits of improved system efficiency through an accelerated boot process via the aid of superior hardware and data compression techniques and taught by Fallon in col. 3, lines 24-40 and col. 4, lines 23-31.

As for claim 37, William's teaches the controller, in response to an address that does not map to the device, converts the address to an address that does map to the device (col. 5 lines 35-56 further discloses by matching address with the configuration registers, one can easily determine the address corresponding to a particular device. For example, if the address does not match address range in a first device, the address is further compared and if it matches address range of the second device, the address is converted to the physical address and chip select of the second device).

He fails however to specifically perform said conversion for a boot code nub that does not match the boot device. Fallon however teaches a system and method for accelerated loading of operating systems and application programs, which stores boot information (boot code nub) in memory devices. The information is loaded and subsequently used to boot the system and load application programs – col. 3, lines 34-52.

As for claim 39, Williams's teaches one device as being coupled to the apparatus via a predetermined chip select line, and each of the remaining devices of the plurality of devices is being coupled to the apparatus via a separate chip select line, and wherein the apparatus activates the predetermined chip select line coupled to the one device, regardless of whether the chip select word is encoded or unencoded (Fig 2, column 6 lines 35-50 teaches the memory device (Fig. 2, element 16A) as being coupled to a predetermined chip select lines CS 1, and the memory device (Fig. 2, element 7A) is coupled to a predetermined chip select lines CS2. Note, Fig. 3 row 2 discloses both unencoded chip select and encoded chip select points to the same physical chip select line.

William's however fails to specifically each said one device as containing the boot code nub as claimed by Applicant.

Fallon however teaches a system and method for accelerated loading of operating systems and application programs, which stores boot information (boot code nub) in memory devices – again, col. 3, lines 34-52.

As for claim 40, Williams teaches a chip select decoder coupled to the apparatus and coupled to each of the devices of the plurality of devices via a separate chip select line, wherein, the chip decoder activates the chip select line of the one device in response to receiving the chip select word, regardless of whether the chip select word is encoded or unencoded. The claim rejected based on the same rationale as of claim 39. Furthermore, in order to generate the physical chip select from encoded chip select and unencoded chip select as showed in Fig. 3, inherently a chip select decoding logic must be employed.

As for claim 42, though William's teaches updating one of the default unencoded chip select mode and the default encoded chip select mode to one of an unencoded chip select mode and an encoded chip select mode (based on the same rationale as claim 41), he fails to teach storing and executing boot hub.

Fallon however teaches a system and method for accelerated loading of operating systems and application programs, which stores boot information (boot code nub) in memory devices – again, col. 3, lines 34-52.

Again, it would have been obvious to one of ordinary skill in the art at the time of the invention for Williams to further include Fallon's system and method for accelerated loading of operating systems and application programs into his own system and method for storing a device row indicator for use in a subsequent page-miss memory cycle. By doing so, Williams could exploit the benefits of improved system efficiency through an accelerated boot process via the aid of superior hardware and data compression techniques and taught by Fallon in col. 3, lines 24-40 and col. 4, lines 23-31.

As for claim 25, Williams's teaches the controller as comprising a memory controller to generate the encoded chip select word and the unencoded chip select word (Fig 1, element 12 illustrates a subsystem controller corresponding to the claim's memory controller to generate the encoded chip select word and the unencoded chip select word (col. 6, lines 13-26)).

As in claim 26, Williams teaches the memory controller as comprising an address decoder to generate the encoded chip select word and the unencoded chip select word (col. 6, lines 18-25, logic to generate encoded row values to be stored in TLB).

As for claim 27, Williams teaches the controller initialization as comprising the configuration of the controller to operate in an encoded chip select mode or in an unencoded chip select mode (col. 6, lines 1-6 teaches the controller as being capable of being configured to operate in encoded chip select mode and/or in unencoded chip select mode).

As for claim 28, Williams teaches the controller as comprising a configuration store to store configuration data to configure the controller to operate in an encoded chip select mode or in an unencoded chip select mode. The claim rejected based on the same rationale as of claim 27. William's column 6 lines 1-6 teaches the controller capable being configured to operated in encoded chip select mode and/or in unencoded chip select mode, therefore inherently the configuration information must be stored in some storage elements in order to convey to the controller the modes in which the controller must be operated on.

As for claim 29, Williams teaches a memory device as per the rejection of claim 24, *supra*.

As for claim 30, Williams teaches the unencoded chip select word as comprising a first bit pattern and the encoded chip select word as comprises a second bit pattern, and the first bit pattern includes the second bit pattern (Fig. 4 illustrates the unencoded chip select word/first bit pattern as including the encoded chip select word/second bit pattern. For example in Fig 4 row 2, the CS 8-1 bit pattern "00000010" includes the CS 2-0 bit pattern "001".

As for claim 31, Williams teaches the lowest order bits of the first bit pattern as including the second bit pattern. William does not expressly disclose the claim's limitation. However, it would have been obvious to one of ordinary skill in the art at the time of the invention for Williams to teach such a pattern. William clearly suggests the controller capable and intent to provide with any encoded bit pattern, any sequential binary values (see William's column 6 lines 2-6). One of ordinary skill in the art would recognize that such a pattern is merely a matter of design choice, and does not render the instant claim patentably distinct from William's disclosure, as both the instant invention and William's disclosures are directed to improving a computer system's programmable chip selection mechanisms.

As for claims 35 and 45, William's teaches the encoded chip select word as being generated according to an encoding scheme to assign numbers to the devices, the numbers to range from one to a number greater than one (col. 5, lines 35-57

teaches using configuration registers that can map an address of any code stored to any memory device, wherein the number of devices to store code can be more that one – see also Fig. 1, element 15).

As for claims 36 and 46, William's teaches the encoded chip select word as encode the number one (Fig. 3 row 1 illustrates encoding the number one as "00000001").

Response to Amendment

5. Applicant's amendments and arguments have been fully considered, but they are moot in view of the new grounds of rejection presented above.

It is worthy to note however that Applicant contends under the heading "Claim Rejections – 35 U.S.C. § 103", that claims 24, 35, 28 and 41 are allowable for including subject matter of claims indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Examiner finds this argument not persuasive, as it is clear that each independent claim, as currently presented, fails to recite each and every element of the claim objected to (including the subject matter of all intervening claims). For example, previous claim 34 (which incorporates subject matter of claims 33 and 24), recites "to generate the unencoded chip select word for the address such that the unencoded chip select comprise exactly one active chip select bit that corresponds to a predetermined chip-select line used to select the boot device". This limitation however is not present in

the currently pending claim 24. As such, Applicant has failed to adopt Examiner's suggestion of rewriting the claims to include the subject matter of all intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

7. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG SOUGH
SUPERVISORY PATENT

10/04/07